## REMARKS/ARGUMENTS

Upon entry of the above amendment, claim 13 will have been canceled without prejudice to or disclaimer of the subject matter recited therein. Claims 11, 14, 20, 21 and 22 will have been amended and resubmitted for consideration by the Examiner. In view of the above, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections of claims in the present application, and submit that such action is now appropriate and proper.

Initially, Applicants would like to express their appreciation to the Examiner for the detailed Official Action provided, and for the acceptance of the drawing filed in the present application on February 7, 2005.

Turning to the merits of the action, claims 11, 18, 21, and 22 were rejected under 35 U.S.C. § 103(a), as being unpatentable over SUZUKI et al. (U.S. Patent No. 5,742,704) in view of ANDREW (U.S. Patent No. 6,904,402) and YANAGIHARA (U.S. Patent No. 5,321,440). Claim 13 was rejected under 35 U.S.C. § 103(a), as being unpatentable over SUZUKI et al. (U.S. Patent No. 5,742,704) in view of ANDREW (U.S. Patent No. 6,904,402), YANAGIHARA (U.S. Patent No. 5,321,440), and PARKER et al. (U.S. Patent No. 6,307,962). Claim 14 was rejected under 35 U.S.C. § 103(a), as being unpatentable over SUZUKI et al. (U.S. Patent No. 5,742,704) in view of ANDREW (U.S. Patent No. 6,904,402), YANAGIHARA (U.S. Patent No. 5,321,440), PARKER et al. (U.S. Patent No. 6,307,962), and ENOKIDA (U.S. Patent No. 5,608,862). Claims 19 and 20 were rejected under 35 U.S.C. § 103(a), as being unpatentable over SUZUKI et al. (U.S. Patent No. 5,742,704) in view of ANDREW (U.S. Patent No. 6,904,402), YANAGIHARA (U.S. Patent No. 5,321,440), and CURRY (U.S. Patent No. 5,710,636).

Claims 15-17 were rejected under 35 U.S.C. § 103(a), as being unpatentable over SUZUKI et al. (U.S. Patent No. 5,742,704) in view of ANDREW (U.S. Patent No. 6,904,402), YANAGIHARA (U.S. Patent No. 5,321,440), and IMAIZUMI et al. (U.S. Patent No. 5,987,176).

As noted above, Applicants have canceled claim 13 and have amended claims 11, 14, 20, 21 and 22. In view of the herein-contained amendments and remarks, Applicants respectfully traverse the above rejections of claims 11 and 13-22, and will discuss said rejections with respect to the pending claims as set forth hereinbelow. The amendments to the claims are not intended to limit or narrow the claimed subject matter, but only to clarify the subject matter recited in the rejected claims.

Applicants' claims 11 and 14-19 generally relate to an image processing apparatus which includes an orthogonal transformer configured to transform multi-bit image data into orthogonal transform coefficients, and a quantizer configured to quantize the orthogonal transform coefficients for each spatial frequency of the multi-bit image data. The spatial frequencies include a DC component, low frequency AC components, and high frequency AC components. A first number of quantization bits is assigned to the DC component, a second number of quantization bits is assigned to all the low frequency AC components, and a third number of quantization bits is assigned to all the high frequency AC components. The second number of quantization bits is a multiple of the first number of quantization bits, and the third number of quantization bits is a multiple of the first number of quantization bits. The image processing apparatus also has a block data generator which generates a block of data. The block of data is composed of the quantized data of each spatial

frequency. Further, the image processing apparatus has a frequency banding section which rearranges the quantized data in the generated block of data so as to band the quantized data of each spatial frequency and so as to align the quantized data of a spatial frequency of the generated block of data with the quantized data of the same spatial frequency of the next generated block of data, and which outputs, as bit serial data, the quantized data of the spatial frequency over a plurality of the rearranged blocks. Moreover, the image processing apparatus has a coder section which compresses the bit serial data, using a coding system for facsimile communication. Claim 20 generally recites a related multifunction apparatus. Claims 21 and 22 generally recite related methods.

In direct contrast to the invention recited in Applicants' claims, SUZUKI et al. relates to an image coding apparatus which produces transform coefficients, quantizes the transform coefficients to produce quantized coefficients each having a predetermined number of bits, converts the quantized coefficients to a one-dimensional string, and constructs coded data by multiplexing into a continuous bit string (Fig. 9, column 8, lines 42-56). SUZUKI et al. teaches that bits are allocated to transform coefficients, according to a fixed bit allocation table shown in Fig. 8A.

However, as admitted in the Official Action, SUZUKI et al. fails to disclose numerous of the above-noted features recited in the present claims. For example, as shown in Figs. 8A-8C of SUZUKI et al., the number of quantization bits allocated to all the low frequency AC components is not a multiple of the number of quantization bits allocated to the DC component, and the number of quantization bits allocated to all the high frequency AC components is not a multiple of the number of quantization bits

allocated to the DC component. Accordingly, in SUZUKI et al., the number of quantization bits allocated to all the low frequency AC components is not a multiple of the number of quantization bits allocated to the DC component, and the number of quantization bits allocated to all the high frequency AC components is not a multiple of the number of quantization bits allocated to the DC component.

In the rejection, the Examiner asserts that "there is only one DC coefficient" and thus the above-noted recitations are satisfied. This is incorrect as the claims refer to the number of bits assigned to the DC component, not to the number of DC coefficients.

SUZUKI et al. also does not disclose a frequency banding section which rearranges the quantized data in the generated block of data so as to band the quantized data of each spatial frequency and so as to align the quantized data of a spatial frequency of the generated block of data with the quantized data of the same spatial frequency of the next generated block of data.

Further, SUZUKI et al. does not disclose a frequency banding section which outputs, as bit serial data, the quantized data of the spatial frequency over a plurality of the rearranged blocks.

Further, Applicants respectfully submit that there is no proper motivation to modify SUZUKI et al. to include the above-noted features recited in Applicants' claims; nor does the outstanding Official Action assert any proper motivation to modify the teachings of SUZUKI to include the above-noted features recited in Applicants' claims. Rather, Applicants respectfully submit that the only motivation to modify SUZUKI in the

manner asserted in the outstanding Official Action is the Examiner's improper motivation to obtain Applicants' claims in hindsight.

In this regard, the prior art does not contain any suggestion to provide SUZUKI with a rearrangement process between a process of generating a one-dimensional string and a coding process. Rather, SUZUKI et el. converts quantized coefficients into a one-dimensional string in order to keep the code amounts constant both when the DCT coding method is applied and when the block truncation coding method is applied (column 8, lines 21-24). Thus, a rearrangement process as recited in the present claims would be merely an extra and meaningless process that would unnecessarily complicate the device of SUZUKI et al.

Additionally, Applicants submit that the Examiner's only assertion of reasons one of ordinary skill in the art would modify SUZUKI et al. to obtain the invention recited in claims 11 and 21 is improper and in error. In this regard, the outstanding Official Action asserts, at page 5, that the necessary modifications to SUZUKI et al. would be obvious "to reduce the coding overhead (as YANAGIHARA indicated in column 1, lines 61-64)". However, YANAGIHARA is only describing the general characteristics of DCT coding in the cited portion of YANAGIHARA. Thus, the above-noted portion of YANAGIHARA is only providing a motivation to use DCT coding, and not a motivation to modify SUZUKI et al. to include the above-noted features of Applicants' claims which SUZUKI et al. does not include. For example, the above-noted motivation would not lead one of ordinary skill in the art to modify SUZUKI et al. to "rearrange the quantized data in the generated block of data so as to band the quantized data of each spatial frequency and so as to align the quantized data of a spatial frequency of the generated

block of data with the quantized data of the same spatial frequency of the next generated block of data, and to output, as bit serial data, the quantized data of the spatial frequency over a plurality of the rearranged blocks" as, e.g., recited in claim 11.

Additionally, since SUZUKI already utilizes DCT, the advantages of DCT, as generally described by YANAGIHARA, would provide no motivation for the modification thereof.

Further, ANDREW does not provide any motivation to modify SUZUKI to obtain the above-noted features of the invention recited in Applicants' claims. Rather, while ANDREW relates to a method that includes rearranging "transform coefficients... into a set of groups", there is no proper motivation to provide the teachings of ANDREW to SUZUKI. Applicants note that the outstanding Official Action does not assert any motivation whatsoever to apply the teachings of ANDREW to SUZUKI; rather, the outstanding Official Action only cites to a portion of YANAGIHARA that discloses the benefits of DCT generally.

Further, even if the teachings of ANDREWS are used to modify SUZUKI, one would still not obtain the invention recited in Applicants' claims. In this regard, ANDREW does not teach that the number of quantization bits assigned to all the low frequency AC components comprises a multiple of the number of quantization bits assigned to the DC component, and does not teach that the number of quantization bits assigned to all the high frequency AC components comprises a multiple of the number of quantization bits assigned to the DC component.

ANDREW also does not disclose a frequency banding section which outputs, as bit serial data, the quantized data of the spatial frequency over a plurality of the

rearranged blocks. Rather, ANDREW merely teaches that the sub-bands of coefficients are coded in turn by the encoder 203 (column 6, lines 56-58), but does not disclose how to input the sub-bands of coefficients into the encoder 203.

Accordingly, even if SUZUKI were modified with the teachings of ANDREW, one of ordinary skill in the art would not obtain the invention recited in Applicants' claims. Accordingly, the pending claims are clearly distinguished over the combination of SUZULI et al. and ANDREW.

Further, Applicants respectfully submit that there is no proper motivation to modify a combination of SUZUKI et al. and ANDREW even further using the teachings of YANAGIHARA et al.; nor has the Examiner asserted any proper motivation to modify a combination of SUZUKI et al and ANDREW according to the teachings of YANAGIHARA et al. In this regard, YANAGIHARA et al. relates to an image encoding apparatus and an image encoding method for encoding image data into sync blocks of fixed length and maximum data volume. YANAGIHARA et al. teaches that, for example, quantizing circuit Q2 quantizes the conversion coefficients disposed within areas 81 and 82 with quantizing step q and conversion coefficients disposed within area 83 with the quantizing step 2q (column 10, lines 5-9).

As noted above, the Official Action asserts that the motivation to modify SUZUKI would have been to reduce the coding overhead (column 1, lines 61-64), as well as to enable selective decoding according to the desired image resolution or quality. However, the portion of YANAGIHARA et al. cited by the Examiner as providing motivation to modify SUZUKI (i.e., column 1, lines 61-64 of YANAGIHARA) merely explains why DCT is useful. In this regard, the cited portion of YANAGIHARA is

entirely silent as to enabling "selective decoding according to the desired image resolution or quality". Thus, Applicants submit that the Official Action has not cited any proper motivation for modifying the combination of SUZUKI et al. and ANDREW with the teaching of YANAGIHARA et al.

Further, YANAGIHARA et al. does not disclose that a first number of quantization bits is assigned to the DC component, a second number of quantization bits is assigned to all the low frequency AC components, a third number of quantization is assigned to all the high frequency AC components, the second number of quantization bits comprising a multiple of the first number of quantization bits, the third number of quantization bits comprising a multiple of the first number of quantization bits. Rather, YANAGIHARA et al. merely teaches that the block 80 of conversion coefficients is divided into different areas, 81, 82 and 83, and each area is associated with a respective quantizing step (column 9, lines 62-65 and column 10, lines 14-23). YANAGIHARA et al. does not disclose or even suggest that the area 81 is assigned to the DC component, the area 82 is assigned to all the low frequency AC components, and the area 83 is assigned to all the high frequency AC components.

Additionally, the Official Action asserts, at page 4, that "applying the same quantization step to both the DC and the AC coefficients implies that the same number of bits is allocated to each quantized coefficients". However, there are no DC or AC coefficients identified in YANAGIHARA. In addition, there is no explanation as to why the Examiner's assertion would be true, nor do Applicants agree that it would be true. In this regard, the outstanding Official Action proceeds to assert that "since there is only one DC coefficient, the total number of bits allocated to all low-frequency (respectively,

high-frequency) quantized AC coefficients is a multiple of the number of bits allocated to the quantized DC coefficient". Applicants respectfully submit that this would only be true if only 1 bit was allocated to the quantized DC coefficient; however, there is no reason to believe this is true. Moreover, based on the use of the term "coefficients" regarding each of areas 81, 82, and 83, it is clearly not true. Accordingly, there is no reason to believe that the total number of allocated bits (both low-frequency and high-frequency) in YANAGIHARA is automatically a multiple of the number of bits allocated to the quantized DC coefficient".

Thus, the pending claims are clearly distinguished over even the combination of SUZUKI et al., ANDREW, and YANAGIHARA et al.

Moreover, as noted above, Applicants respectfully submit that there is no motivation to modify the combination of SUZUKI et al. and ANDREW, with the teaching of YANAGIHARA et al. In particular, there is no motivation to provide SUZUKI et al. with the teachings of the secondary references to have the quantizer recited in the pending claims, as the quantizer recited in the pending claims would merely complicate SUZUKI et al. with an extra and meaningless process.

Further, there is no motivation to apply the teachings of YANAGIHARA to the disclosure of SUZUKI. Additionally, as shown above, even the combination of teachings of YANAGIHARA to modify SUZUKI would not result in the invention recited in Applicants' claims, as YANAGIHARA does not disclose that the numbers of quantization bits assigned to the low frequency AC components and assigned to the low frequency components would be a "multiple" of the number of bits assigned to the DC component. Accordingly, Applicants respectfully submit that the Examiner has not

set forth any proper motivation for modifying SUZUKI et al. with the teaching of YANAGIHARA et al.

Thus, Applicants respectfully submit that there is no motivation to modify the teachings of SUZUKI with the teachings of ANDREW and/or YANAGIHARA. Further, Applicants respectfully submit that even the combined teachings of SUZUKI, ANDREW and/or YANAGIHARA would not result in the above-noted combinations of features recited in Applicants' independent claims 11, 20 and 21. Accordingly, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections that is based on the above-noted combinations of SUZUKI, ANDREW and YANAGIHARA.

Applicants would like to further explain the features of the present invention, in order to emphasize the differences between the claimed invention and the teachings of the references applied in the Official Action. In this regard, the present invention relates to compressing bit serial data, using a coding system for facsimile communication, such as, for example, a JBIG coding system. The coding system for facsimile communication increases compression efficiency as the number of successive dots of white and black is getting larger in dimension (page 12, lines 20-27). Thus, the present invention provides additional processes (for example, a block data generation process and a rearrangement process) between a quantizing process and a coding process. For the present invention, these extra processes increase the compression efficiency in the coding system for facsimile communication, since these additional processes make the number of successive dots of white and black larger, before compressing data. Further, the present invention compresses binary data which

consists of white data and black data, since the present invention relates to using a coding system for facsimile communication, such as, for example, a JBIG coding system.

On the other hand, YANAGIHARA et al. relates to a digital video tape recorder (DVTR) (column 3, lines 23-24, column 6, lines 31-37). In other words, YANAGIHARA et al. adopts a coding system for color data. Thus, YANAGIHARA et al. does not adopt a coding system (for example, a J-BIG coding system) which increases compression efficiency as the number of successive dots of white and black is getting larger in dimension. Thus, for this additional reason, there is no motivation for modifying SUZUKI et al. with the teaching of YANAGIHARA to obtain the pending claims.

As noted above, the Examiner has not set forth a proper motivation for combining SUZUKI et al., ANDREW, and YANAGIHARA et al. In this regard, SUZUKI et al., ANDREW and YANAGIHARA et al. are not all even directed to the same protocols and systems. Merely because references are from a same field of endeavor is not a sufficient or adequate reason to conclude that the references are combinable. Accordingly, the only motivation to modify SUZUKI in the manner asserted by the Examiner is the impermissible motivation of the Examiner to obtain Applicants' claims in hindsight.

Applicants further submit that none of the other references applied in the Official Action discloses the above-noted features recited in Applicants' claims. Further, the outstanding Official Action has not asserted any proper motivation to modify the teachings of SUZUKI with the teachings of PARKER.

In particular, PARKER et al. discloses a standard fax coding (Fig.1, ref. 18, column 6, lines 52-56). However, PARKER et al. does not disclose the recited quantizer, the recited block data generator, or the recited frequency banding section. In other words, PARKER et al. does not disclose any processes for increasing the compression efficiency in the coding system for facsimile communication, before compressing data. Thus, there is no proper reason to modify the teachings of SUZUKI with the teachings of PARKER et al.

Therefore, it is respectfully submitted that the features recited in Applicants' independent claims 11, 20 and 21, and dependent claims 14, 15-19 and 22 are not disclosed in PARKER et al. cited by the Examiner.

Accordingly, the pending claims are submitted to be patentable over the Examiner's proposed combination. Accordingly, at least for each of the numerous reasons set forth above, Applicants respectfully request reconsideration and withdrawal of the rejections of each of claims 11, 20 and 21. Applicants further submit that dependent claims 14-19 are allowable at least for depending, directly or indirectly, from an allowable independent claim, as well as for additional reasons related to their own recitations.

## SUMMARY AND CONCLUSION

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so. Applicants have amended the rejected claims and resubmitted the same for consideration by the Examiner. Further, Applicants have provided a clear evidentiary basis supporting the patentability of all claims in the present application and respectfully request an indication of the allowability of all the claims pending in the present application in due course.

Applicants note that this amendment is being made to advance prosecution of the application to allowance, and with respect to the claimed features argued as deficient in the prior art, should not be considered as surrendering equivalents of the territory between the claims prior to the present amendment and the amended claims. Further, no acquiescence as to the propriety of the Examiner's rejection is made by the present amendment.

All amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should the Examiner have any questions or comments regarding this Response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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